# DR. HARSUPREET KAUR


## Associate Professor

Department of Electronic Science, University of Delhi South Campus
Benito Juarez Road, New Delhi – 110 021


## PROFILE

**Harsupreet Kaur** (SM'18) received the B.Sc. (Hons.) and M.Sc. degrees in Physics and the Ph.D. degree in Electronics from the University of Delhi, New Delhi, India, in 2001, 2003, and 2008, respectively. She is currently an Associate Professor at the Department of Electronic Science, University of Delhi. Her current research interests include modeling, design, and simulation of advanced semiconductor devices.

## CONTACT


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https://electronics.du.ac.in/docs/ElectSci_Harsupreet_final.pdf

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## AREAS OF INTEREST

Modeling, design and simulation of Advanced Semiconductor Devices, MultiGate FETs, Junctionless devices, Negative capacitance devices, $Ga_2O_3$ devices

## EDUCATION

Ph.D., University of Delhi, 2008

Thesis Title: Modeling and Simulation of Channel and Gate Oxide Engineered Cylindrical/Surrounding Gate MOSFETs for ULSI Applications.

M.Sc. Physics, Dept. of Physics and Astrophysics, University of Delhi, 2001-2003

B.Sc. (H) Physics, University of Delhi, 1998-2001

## WORK EXPERIENCE

Associate Professor, Dept. of Electronic Science, University of Delhi (April 2021 till date)

Assistant Professor, Dept. of Electronic Science, University of Delhi (2013-2021)

Assistant professor (Adhoc), Bhaskaracharya College of Applied Sciences, University of Delhi (2011-2013)

Assistant professor (Adhoc), Deen Dayal Upadhyaya College, University of Delhi, University of Delhi (2009-2011)

Lecturer (Adhoc), Acharya Narendra Dev College, University of Delhi (2007-2009)

## PUBLICATION PROFILE

Total Articles: 113, h – index: 11, i10 index: 11 (Google Scholar)

In International Journals: 32 In International Conferences: 76
In National conferences - 05

## RESEARCH PROJECTS

Total (Minor): 05
Funding Agency: University of Delhi, Institute of Eminence (DU)

## AWARDS/ DISTINCTIONS

Young Scientist Award' in The XXIX General Assembly of the International Union of Radio Science (Union Radio-Scientifique Internationale) URSI-GA 2008 conference held in Chicago, Illinois, USA during August 7-16, 2008.

## CONFERENCE/WEBINAR ORGANIZED

Conferences – 08 (Roles: Co-Chair – 03, As Member OC/LOC/ TPC -05)

Workshops/ Seminars – 19 (Coordinator)

## PH.D. SUPERVISION

Awarded: 03 (Sole supervision) Under Progress - 01

## MEMBERSHIPS OF PROFESSIONAL BODIES

- Senior Member, IEEE USA (June 2018)
- Member, Electronic Devices Society, USA
- Member -IEEE Solid-State Circuits Society
- Life Member - Semiconductor Society of India
- Secretary - IEEE EDS Delhi Chapter (Jan 2020 – till date)

# Dr. Harsupreet Kaur


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|---|---|
| Designation | **Associate Professor** |
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## EDUCATIONAL QUALIFICATIONS

| | | |
|---|---|---|
| Ph.D. | **University of Delhi** | **2008** |
| PG (M.Sc Physics) | **University of Delhi** | **2003** |
| UG (B.Sc (H) Physics) | **University of Delhi** | **2001** |

## CAREER PROFILE

| Organization | Designation | Duration |
|---|---|---|
| **Department of Electronic Science, UDSC** | **Associate Professor** | **April 08, 2021 till date** |
| **Department of Electronic Science, UDSC** | **Assistant Professor** | **April 01, 2013- April 07, 2021** |
| **Bhaskaracharya College of Applied Sciences,University of Delhi** | **Assistant Professor** | **2011- April 2013 (Ad-hoc)** |
| **Deen Dayal Upadhyaya College, Universityof Delhi** | **Assistant Professor** | **2009-2011 (Ad-hoc)** |
| **Acharya Narendra Dev College, Universityof Delhi** | **Lecturer/Assistant Professor** | **2007- 2009 (Ad-hoc)** |

## ADMINISTRATIVE ASSIGNMENTS

**Head – Dept. of Electronic Science (March 2023 - )**
**Member – Academic Council (March 2023 -)**
**Member -Standing Committee on Academic Matters (March 2023 -)**
**Warden – Geetanjali Hostel, University of Delhi South Campus (December 2022 till date)**
**Superintendent – Theory exams of post graduate courses - South Campus – May-June 2023**
**Coordinator/Co-Coordinator - Committee for undergraduate courses (For B.Sc.(H) Electronics/ Instrumentation courses running in 13 undergraduate colleges of Delhi University) (2013 till March 2023)**
**Convenor/ Member - Library Committee (2013-2023)**
**Member- Department Purchase Committee (2019-till date)**
**Member – Department Research Committee (2013 till date)**
**Member – Committee of Courses (2013 till date)**
**Convenor/ Member - Student Grievance committee (2017-till date)**
**Member – COVID-19 Task committee (2020-2022)**
**Member – M.Sc. Electronics Syllabus revision committee (2018-2019)**
**Election Officer - South Delhi Campus Students Union Elections (2016-2019)**
**Member – Faculty of Interdisciplinary Sciences, UDSC (2013-16)**
**Member - Board of Research Studies (BRS, (FIAS, DU) (2013-2015, 2017-2019, 2021 till date))**
**Nodal Officer - Dept. of Electronic Science for NAAC (2013-2018)**
**Nodal officer for foreign students for Dept. of Electronic Science (2016-2017, 2018-2019)**
**Member - TIC CLUB, Electropreneur Park, University of Delhi South Campus (2016-2017).**

## AREAS OF INTEREST:

- Modeling, Design and Simulation of Novel and Advanced Semiconductor Devices.
- VLSI Circuit Design and Device Modeling
- Negative Capacitance devices

## SUBJECTS TAUGHT

M.Sc Electronics

Theory Papers: Network Analysis and Synthesis, Analog CMOS Circuit Design, VLSICircuit Design and Device Modeling,

Laboratory classes: Electronic Circuits, Circuit Design and simulation

Ph.D (Electronic Science)

Coordinator - Research methodology paper (2016 - till date)

## RESEARCH GUIDANCE

1. *Supervision of awarded Doctoral Thesis* – 03 (Sole supervision)
2. *Supervision of Doctoral Thesis, under progress* – 01
3. *Supervision of M.Sc Major projects*- 47 (Work of some of these has resulted in the following papers in International conferences):
    - P. Goel and Harsupreet Kaur, “Assessing the Suitability of DMG-HK Trapezoidal FinFET for High Temperature Applications”, 4th International Conference on Microelectronics and Telecommunication Engineering (ICMETE 2020), 26-27 September, 2020
    - P. Goel and Harsupreet Kaur, “Superior Performance of Gate Workfunction and Gate Dielectric Engineered Trapezoidal FinFET in the presence of Trap Charges, 7th International Conference on Microelectronics, Circuits and Systems (MICRO 2020), 25- 26 July, 2020
    - Somishang Jagoi, Divya Pawar and Harsupreet Kaur, "Efficacy of Non-Uniformly Doped and Multi-layered Gate Dielectric Designs in Improving Device Perfomance of Elliptical MOSFETs", Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) held at SRM University, Delhi- NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018.
    - Priyanka Pandey, Pooja Puri and Harsupreet Kaur, “Dual Material Gate-Gate Stack-Elliptical Gate All Around (DMG-GS-EG) MOSFET– A Novel Device Concept for Improved Performance”, International Conference on Advances in Electronics, Computers and Communications (ICAECC 2018) held at Reva University, Bangalore, India, 9$^{th}$-10$^{th}$ February 2018.
    - Monika Bansal and Harsupreet Kaur, “Analytical Threshold Voltage Model to study the impact of Graded-Channel (GC) design and gate dielectric engineering on device performance of Tri-Gate MOSFET”, presented (ORAL) in International Conference on Recent Innovations in Engineering and Technology (ICRIEAT 2016), held at Hotel Katriya, Hyderabad, India, 22$^{nd}$-23$^{rd}$ December 2016.
    - Harsupreet Kaur, Hema Mehta, "Analytical Modeling of Gate Oxide Engineered Junctionless SOI MOSFET with Vertical Gaussian-like Doping Profile", ICMARS 2014, 9-12 Dec 2014, Jodhpur, India.

## PUBLICATION PROFILE

### RESEARCH PAPERS PUBLISHED IN SCOPUS INDEXED/ SCIE JOURNALS

1. Priyanshi Goyal and Harsupreet Kaur, “Assessing the impact of step gate oxide and gate electrode engineering on performance of β-$Ga_2O_3$ MOSFET for high frequency applications”, Micro and Nanostructures 180, 207603.
2. Priyanshi Goyal and Harsupreet Kaur, “Impact of Dual Material Gate Design and Retrograde Channel Doping on β- $Ga_2O_3$ MOSFET for High Power and RF Applications”, Silicon 15 (4), 1597-1608.
3. Priyanka Pandey and Harsupreet Kaur, “Investigation of palladium gated polarity controllable FET as a highly sensitive and robust hydrogen gas sensor”, International Journal of Numerical Modelling: Electronic Networks, Devices and Fields”.
4. Priyanshi Goyal and Harsupreet Kaur, “Exploring the efficacy of implementing field plate design with air gap on β-Ga2O3 MOSFET for high power & RF applications”, Micro and Nanostructures 173, 207454.
5. Priyanka Pandey and Harsupreet Kaur, “Exploring the Performance of Palladium gated–SiGe channel–polarity controllable–FET for hydrogen gas monitoring applications”, Micro and Nanostructures 169, 207357.
6. Priyanshi Goyal and Harsupreet Kaur, “Implementing variable doping and work function engineering in β-$Ga_2O_3$ MOSFET to realize high breakdown voltage and PfoM”, Semiconductor Science and Technology, 14;37(4):045018. (2022)
7. Priyanka Pandey and Harsupreet Kaur, “Performance investigation of Reconfigurable–FET under the influence of parameter variability of ferroelectric gate stack at high temperatures”, Microelectronics Journal, Volume 124, 105442, 2022.
8. Priyanka Pandey and Harsupreet Kaur, “A comprehensive physics based surface potential and drain current model for SiGe channel dual programmable FETs” Semicond. Sci. Technol. 2022, 37 055017
9. Priyanka Pandey and Harsupreet Kaur, “Performance and sensitivity analysis of polarity controllable-Ion sensitive FET for pH sensing applications. Silicon (2022) DOI:10.1007/s12633-022-01658-y.
10. Priyanka Pandey and Harsupreet Kaur, “Effect of ferroelectric parameters variation on the characteristics of polarity controllable–ferroelectric–field-effect transistors at elevated temperatures”, Semiconductor Science and Technology, Volume 35, Number 12, 2020.
11. Monika Bansal and Harsupreet Kaur, “Device and Circuit Level Analysis of Negative Capacitance Hybrid CMOS: A Prospect for Low Power/Low Voltage Applications,” Semiconductor Science and Technology, vol. 35, no. 1, pp. 015014, Jan. 2020. DOI: 10.1088/1361-6641/ab57b4
12. Priyanka Pandey and Harsupreet Kaur, “Improved Temperature Resilience and Device Performance of Negative Capacitance Reconfigurable Field Effect Transistors”, IEEE Transactions on Electron Devices,Vol. 67 No. 2, 2019. DOI:10.1109/TED.2019.2961876.
13. Hema Mehta and Harsupreet Kaur, "Performance Assessment of Symmetric Double Gate Negative Capacitance Junctionless Transistor with High-k Spacer at Elevated Temperatures", Advances in Natural Sciences: Nanoscience and Nanotechnology Jointly Published by VAST

(VN)and IOP (UK) vol. 10, no. 3, pp. 035013, Sept. 2019. DOI: 10.1088/2043-6254/ab3d2e

14. Hema Mehta and Harsupreet Kaur , "Superior Performance and Reliability of Double Gate Gaussian Doped Negative Capacitance Junctionless Transistor for 200–500 K", IETE Technical Review, July 2019. DOI: 10.1080/02564602.2019.1642149.
15. Hema Mehta and Harsupreet Kaur, "Study on Impact of Parasitic Capacitance on Performance of Graded Channel Negative Capacitance SOI FET at High Temperature" IEEE Trans. Electron Devices, vol. 66, no 7, pp. 2904-2909, Jul. 2019. DOI: 10.1109/TED.2019.2917775
16. Hema Mehta and Harsupreet Kaur, "Subthreshold Analytical Model for Dual-Material Double Gate Ferroelectric Field Effect Transistor (DMGFeFET))" Semiconductor Science and Technology, vol. 34, pp. 065008, 2019, DOI: 10.1088/1361-6641/ab194d
17. Monika Bansal and Harsupreet Kaur. Analysis of Negative-Capacitance Germanium FinFET With the Presence of Fixed Trap Charges, IEEE Transactions on Electron Devices, 66(4), 2019, 1979 - 1984
18. Monika Bansal and Harsupreet Kaur, "An analytical subthreshold current model for ferroelectric SiGe-on-insulator field effect transistor (FSGOIFET)" Semiconductor Science and Technology, Vol.34, no.1, December 2018.
19. Hema Mehta and Harsupreet Kaur, "Impact of Gaussian Doping Profile and Negative Capacitance Effect on Double Gate Junctionless Transistors (DGJLT)" IEEE Trans. Electron Devices, vol. 65, no. 7, pp. 2699–2706, Jul. 2018. DOI: 10.1109/TED.2018.2832843.
20. Monika Bansal and Harsupreet Kaur, "Impact of negative capacitance effect on Germanium Double Gate pFET for enhanced immunity to interface trap charges" Superlattices and Microstructures, vol. 117, pp. 189-199, 2018, DOI: 10.1016/j.spmi.2018.03.001.
21. Hema Mehta and Harsupreet Kaur, "Impact of interface layer and metal workfunction on device performance of ferroelectric junctionless cylindrical surrounding gate transistors" Superlattices and Microstructures, DOI: 10.1016/j.spmi.2017.06.032.
22. Hema Mehta and Harsupreet Kaur, "High temperature performance of Si:HfO2 based long channel Double Gate Ferroelectric Junctionless Transistors" Superlattices and Microstructures, vol. 103, pp. 78-84, 2017.
23. Hema Mehta and Harsupreet Kaur, "Modeling and simulation study of novel Double Gate Ferroelectric Junctionless (DGFJL) transistor" Superlattices and Microstructures, vol. 97, pp. 536-547, 2016
24. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Graded Channel (GC) design in fully depleted cylindrical/surrounding gate MOSFET (FD CGT/SGT) for improved short channel immunity and hot carrier reliability" Solid State Electronics, vol. 51, pp.398-404, 2007.
25. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, An analytical drain current model for graded channel cylindrical/surrounding gate MOSFET, Microelectronics Journal, vol.38, pp.352-359, 2007.
26. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "An Analytical Threshold Voltage Model for Graded Channel Asymmetric Gate Stack (GCASYMGAS) Surrounding Gate MOSFET" Solid State Electronics, vol. 52, pp.305-311, 2008.
27. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Laterally Asymmetric Channel and Gate Stack Design on Device Performance of Surrounding Gate MOSFETs : A Modeling and Simulation Study", Vol. 52, no. 3, pp. 746-750, 2010 Microwave and Optical Technology Letters
28. Sneha Kabra, Harsupreet Kaur, Ritesh Gupta, Subhasis Haldar, Mridula Gupta and R.S.Gupta "A Semi Empirical Approach for Submicron GaN MESFET Using an Accurate Velocity Field Relationship for High Power Applications", Microelectronics Journal, vol. 37, no.7, pp.620-626,

2006.

29. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta, "Temperature Dependent Analytical Model of sub-micron GaN MESFETs for Microwave frequency Applications", Vol. 52, no. 1, 25-30, 2008, Solid State Electronics.
30. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta "An Analytical Model for GaN MESFET's Using New Velocity-Field Dependence" Physica Status Solidi C, vol. 3, no. 6, pp. 2350-2355, 2006.
31. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta, "Two Dimensional Subthreshold Analysis of Sub-Micron GaN MESFET" Microelectronics Journal, vol. 38, no. 4-5, pp. 547–555, 2007.
32. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta, "A Semi-Empirical Model for Admittance and Scattering Parameters of GaN MESFET for microwave circuit applications" Volume 49, Issue 10, October 2007, Pages: 2446-2450, Microwave and optical technology Letters.

**INTERNATIONAL CONFERENCES**

1 Priyanshi Goel and Harsupreet Kaur, "Implementation of Step-Hetero-Oxide & Dual material Gate Designs on Lateral β-$Ga_2O_3$ MOSFET for Terahertz Applications" IEEE Latin American Electron Devices Conference (LAEDC) 2023, July 3-5, 2023.

2 Priyanshi Goel and Harsupreet Kaur, "TCAD Investigation of Step-Oxide and Asymmetric Doping Design with Electrode Engineering on Lateral β-Ga2O3 MOSFET for Terahertz Applications" IEEE Latin American Electron Devices Conference (LAEDC) 2023, July 3-5, 2023.

3 Priyanshi Goel and Harsupreet Kaur, "Performance Evaluation of Gaussian Doped & Work Function Engineered Lateral β-$Ga_2O_3$ MOSFET for High Power RF Applications. *2022* IEEE International Women in Engineering (WIE) Conference on Electrical and Computer Engineering (WIECON-ECE) (pp. 208-211). IIIT-Naya Raipur (hybrid mode), India, 30-31 Dec. 2022.

4 Priyanshi Goel and Harsupreet Kaur, "Effect of Step Doping Profile and Dual Material Gate Design on β-Ga2O3 for superior RF Performance", 6th IEEE International Conference on Devices, Circuits and Systems (ICDCS) 2022 (pp. 6-10).

5 Goyal P, Kaur H. Impact of Vertically Graded (VGrad) channel design on device performance of β-Ga2O3 MOSFET.IEEE 2022 7th International Conference for Convergence in Technology (I2CT),Pune, Maharashtra, 7th- 8th April,2022. (Hybrid Mode).

6 P. Pandey and H. Kaur, "Analysis of pH sensing performance of polarity controllable-ferroelectric-ion sensitive FET", in proc. 8th IEEE International WIE Conference on Electrical and Computer Engineering (WIECON-ECE), IIIT-Naya Raipur (hybrid mode), India, 30-31 Dec. 2022.

7 P. Pandey and H. Kaur, "Performance investigation of polarity controllable-ferroelectric-FET for hydrogen gas sensing applications", 8th IEEE International WIE Conference on Electrical and Computer Engineering (WIECON-ECE), IIIT-Naya Raipur (hybrid mode), India, 30-31 Dec. 2022.

8 P. Pandey and H. Kaur, Impact of Mole Fraction Variation on the pH Sensing Performance of SiGe channel based Polarity Controllable Ion Sensitive FET – Part-I, 2022 IEEE 7th International Conference for Convergence in Technology (I2CT), Pune, India, 7-9 April 2022. DOI: 10.1109/I2CT54291.2022.9824400. Electronic ISBN: 978-1-6654-2168-3.

9 P. Pandey and H. Kaur, Impact of Mole Fraction Variation on the pH Sensing Performance of SiGe channel based Polarity Controllable Ion Sensitive FET – Part-II, 2022 IEEE 7th International Conference for Convergence in Technology (I2CT), Pune, India, 7-9 April 2022. DOI: 10.1109/I2CT54291.2022.9824897. Electronic ISBN: 978-1-6654-2168-3.

10 Goyal P, Kaur H. Exploring the suitability of Dual Step Gate Oxide Design on β – $Ga_2O_3$ MOSFET for High Power Microwave Applications – Part I, Latin American Electron Devices Conference (LAEDC) - 4th- 6th July,2022 (Hybrid Mode)

11 Goyal P, Kaur H. Exploring the suitability of Dual Step Gate Oxide Design on β – $Ga_2O_3$ MOSFET for High Power Microwave Applications – Part II.Latin American Electron Devices Conference (LAEDC) - 4th- 6th July,2022 (Hybrid Mode)

12 Priyanka Pandey and Harsupreet Kaur, "Improved device performance of polarity controllable– ferroelectric–field effect transistor under the influence of fixed trap charges", *2021 IEEE Latin America Electron Devices Conference (LAEDC),* Mexico, 19-21 April 2021. DOI: 10.1109/LAEDC51812.2021.9437921. Electronic ISBN:978-1-6654-1510-1.

13 Priyanka Pandey P and Harsupreet Kaur, "Improved Device Performance of Polarity Controllable Ferroelectric Field Effect Transistor Under the Influence of Fixed Trap Charges", 3rdLatin American Electron Devices Conference LAEDC 2021, held during April 19- 21, 2021.

14 Priyanshi Goel and Harsupreet Kaur, "Analytical Modeling and Design of $Ga_2O_3$ MOSFET", 5th IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE) held during December 1-3, 2020.

15 Priyanshi Goel and Harsupreet Kaur, "Assessing the Suitability of DMG-HK Trapezoidal FinFET for High Temperature Applications", 4th International Conference on Microelectronics and Telecommunication Engineering (ICMETE 2020), 26-27 September, 2020

16 Priyanka Pandey and Harsupreet Kaur, "High Temperature Analysis of Negative Capacitance–Reconfigurable–FET Under the Impact of Ferroelectric Parameters Variation", 7th International Conference on Microelectronics, Circuits and Systems (MICRO 2020), 25-26 July, 2020.

17 Priyanshi Goel and Harsupreet Kaur, "Superior Performance of Gate Workfunction and Gate Dielectric Engineered Trapezoidal FinFET in the presence of Trap Charges, 7th International Conference on Microelectronics, Circuits and Systems (MICRO 2020), 25-26 July, 2020.

18 Priyanka Pandey and Harsupreet Kaur, "High Temperature Analysis of Negative Capacitance–Reconfigurable–FET Under the Impact of Ferroelectric Parameters Variation, 7th International Conference on Microelectronics, Circuits and Systems (MICRO 2020), 25-26 July, 2020

19 Priyanka Pandey and Harsupreet Kaur, "Performance Assessment of Polarity Tunable–Ferroelectric–Field Effect Transistor at High Temperature —Part I", IEEE 5thInternational Conference on Devices, Circuits and Systems (ICDCS -2020), Coimbatore, 5-6Mar. 2020.

20 Priyanka Pandey and Harsupreet Kaur, "Performance Assessment of Polarity Tunable–Ferroelectric–Field Effect Transistor at High Temperature —Part II", IEEE 5thInternational Conference on Devices, Circuits and Systems (ICDCS -2020), Coimbatore, 5-6Mar. 2020.

21 Priyanka Pandey and Harsupreet Kaur,Enhanced Reliability of Polarity Controllable–Ferroelectric– FETs under the Impact of Fixed Trap Charges, Springer 3rdInternational Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, 28-29Sept. 2019

22 Priyanka Pandey and Harsupreet Kaur,Effect of SBT Ferroelectric Layer on Polarity ControllableFETs for Improved Current Drivability, IEEE 16thINDICON 2019, Gujrat, 13-15Dec. 2019.

23 Priyanka Pandey and Harsupreet Kaur,Impact of Fixed Trap Charges on the Device

Performance of Polarity Controllable–Ferroelectric–Field Effect Transistor, IEEE 20thInternational Workshop on Physics of Semiconductor Devices(IWPSD-2019), Kolkata, 17-20Dec. 2019.

24 H. Mehta and H. Kaur, "Junctionless Gaussian Doped Negative Capacitance SOI Transistor: Investigation of Device Performance for Analog and Digital Applications," International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, Uttar Pradesh, India, 2019.

25 M. Bansal and H. Kaur, "Circuit Analysis of Pass Transistors and Inverter based on Negative Capacitance Silicon-Germanium Double Gate FET (NCSiGeDGFET)," in Proc. IEEE Global Conference for Advancement in Technology (GCAT), Bangalore, India, 18th-20th October 2019.

26 M. Bansal and H. Kaur, "Study to find the applicability of Germanium FinFET with Negative Capacitance for High Temperatures Applications", IEEE International Conference on Signal Processing, Computing and Control (ISPCC), Solan, India, 10th-12th October 2019

27 M. Bansal and H. Kaur, "Study to Analyze the Impact of Fixed Trap Charges on the Performance of Germanium Ferroelectric Double Gate FET (GeFeDGFET)," IEEE International Conference On Computing, Power and Communication Technologies (GUCON), Greater Noida, Uttar Pradesh, India,27th-28th September 2019.

28 Priyanka Pandey and Harsupreet Kaur," Surface Potential Model for Ferroelectric Nanowire Field Effect Transistor with NiSi2 Source/Drain", IEEE International Conference on Emerging Electronics (ICEE) 2018 held at Royal Orchid Resort and Convention Centre, Bangalore, India, 16th- 19th December 2018.

29 Monika Bansal and Harsupreet Kaur, "Ferroelectric GeSn On Insulator FET: Device and Circuit Analysis for Steep Switching Applications", IEEE International Conference on Emerging Electronics (ICEE) 2018 held at Royal Orchid Resort and Convention Centre, Bangalore, India, 16th- 19th December 2018.

30 Priyanka Pandey and Harsupreet Kaur, "Impact of SBT Ferroelectric layer on Reconfigurable FETs for Steep Switching Characteristics and Improved Performance", IEEE 4th International Conference for Convergence in Technology (I2CT), SDMIT Mangalore, 27-28 October 2018.

31 Priyanka Pandey and Harsupreet Kaur, "Drain Current Model of Reconfigurable Ferroelectric Field Effect Transistor (R-Fe-FET)", IEEE 4th International Conference for Convergence in Technology (I2CT), SDMIT Mangalore, 27-28 October 2018.

32 Somishang Jagoi, Divya Pawar and Harsupreet Kaur, "Efficacy of Non-Uniformly Doped and Multi- layered Gate Dielectric Designs in Improving Device Perfomance of Elliptical MOSFETs", SecondIEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) held at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21, September 2018.

33 Monika Bansal and Harsupreet Kaur, "Impact of Ferroelectric Material Properties on Device Characteristics of Ferroelectric Ge0.97Sn0.03 Double Gate FET (FEGeSnDGFET)", in IEEE International Microwave and RF Conference (IMaRC) 2018 to be held at Bharati Hotel Novotel, Kolkata, India, 28th-30th November 2018.

34 Hema Mehta and Harsupreet Kaur, "Performance Assessment of Symmetric Double Gate Negative Capacitance Junctionless Transistor with High-k Spacer at Elevated Temperatures" in NANOCON-2018 International Conference on Nanotechnology, to be held at, Bharati

Vidyapeeth University, Pune, Maharahstra, from October 25-26, 2018.

35 Monika Bansal and Harsupreet Kaur, "Superior Device Performance and Reliability of Germanium Ferroelectric Double Gate FET (GeFeDGFET) at High Temperatures", in NANOCON 2018 to be held at Bharati Vidyapeeth University, Pune-Satara Road Campus, Pune, India, 25th- 26th October 2018.

36 Monika Bansal and Harsupreet Kaur, "Ferroelectric-Insulator-Germanium Double Gate (F-I-GeDG) FET with steep switching characteristics and improved current drivability", in IEEE International Conference On Computing, Power And Communication Technologies 2018 (GUCON) held at Radisson Blu Hotel, Greater Noida, Uttar Pradesh, India, 28th-29th September2018.

37 Monika Bansal and Harsupreet Kaur, "Improvement in switching characteristics of Ferroelectric- Insulator-Germanium Double Gate (F-I-GeDG) FET for ultra low power applications", in IEEE International Conference On Computing, Power And Communication Technologies 2018 (GUCON) held at Radisson Blu Hotel, Greater Noida, Uttar Pradesh, India, 28th-29th September 2018.

38 Hema Mehta and Harsupreet Kaur, "Impact of Ferroelectric HfO2 and Non-Uniform Doping on Nanoscale Planar SOI Junctionless Transistor" in GUCON-2018 IEEE International Conferenceon Computer, Power and Communication Technologies, held at, Radisson Blu Hotel, Greater Noida, Uttar Pradesh, from September 28-29, 2018.

39 Hema Mehta and Harsupreet Kaur, "Double Gate Graded Channel Negative Capacitance FET (DGGCNCFET): Performance Assessment for Low Power Digital/Analog Applications" in GUCON- 2018 IEEE International Conference on Computer, Power and Communication Technologies, held at, Radisson Blu Hotel, Greater Noida, Uttar Pradesh, from September 28-29, 2018.

40 Monika Bansal and Harsupreet Kaur, "Negative Capacitance Germanium-Double Gate FET- A novel device concept for ultra low voltage/low power applications", in International Conference on Control, Communication and Computing 2018 (IC4) held at College Of Engineering, Trivandrum, Kerala, India, 5th-7th July 2018.

41 Monika Bansal and Harsupreet Kaur, "Performance investigation of Negative Capacitance Germanium Double Gate-pFET (NCGe-DG-pFET) for improved analog applications", presented (ORAL) in IEEE International Symposium on Devices, Circuits and Systems (ISDCS) held at IIEST, Shibpur, Kolkata, India, 29th-31st March 2018.

42 Hema Mehta and Harsupreet Kaur, "Impact of High-k spacer and Negative Capacitance on Double Gate Junctionless Transistor for Improved Short Channel Immunity and Reliability" in ICDCS-2018 IEEE International Conference on Devices, Circuits and Systems (ICDCS'18), held at, Karunya Institute of Technology and Sciences, India, from March 16-17, 2018.

43 Hema Mehta and Harsupreet Kaur, "Performance Study of Short Channel Symmetric Double Gate Gaussian Doped Ferroelectric FET for Analog and Digital Applications" in ICDCS-2018 IEEE International Conference on Devices, Circuits and Systems (ICDCS'18), held at, Karunya Institute of Technology and Sciences, India, from March 16-17, 2018.

44 Monika Bansal and Harsupreet Kaur, "Analytical drain current model to study the impact of interface trap charges on device performance of Double Gate Ge Ferroelectric FET (DGGeFeFET)", presented (ORAL) in 3rd IEEE International Conference on Emerging Devices and Smart Systems (ICEDSS) held at Mahendra Engineering College, Namakkal DT, Tamilnadu,

India,2nd-3rd March 2018.

45 Priyanka Pandey, Pooja Puri and Harsupreet Kaur, "Dual Material Gate-Gate Stack-Elliptical Gate All Around (DMG-GS-EG) MOSFET– A Novel Device Concept for Improved Performance", International Conference on Advances in Electronics, Computers and Communications (ICAECC 2018) held at Reva University, Bangalore, India, 9th-10th February 2018.

46 Hema Mehta and Harsupreet Kaur, "Impact of Negative Capacitance Effect and Graded ChannelDesign on Device Performance of Double Gate MOSFET",XIX International Workshop on The Physics of Semiconductor Devices (IWPSD 2017), held at IIT Delhi, December 11-15, 2017.

47 Hema Mehta and Harsupreet Kaur, "Temperature Dependent Analytical Model for Cylindrical Surrounding Gate Ferroelectric Junctionless Transistor (CSGFJL)", in XIX International Workshopon The Physics of Semiconductor Devices (IWPSD 2017), held at IIT Delhi, India, from December11-15, 2017.

48 Hema Mehta and Harsupreet Kaur, "Double Gate Gaussian Doped Negative Capacitance FET (DGGDNCFET): A Novel Concept for Enhanced Device Performance in INDICON-2017 14TH IEEE India Council International Conference 2017, held at, IIT Roorkee, India, from December 15-17, 2017.

49 Hema Mehta and Harsupreet Kaur, "Design Space Optimization for Nanoscale Graded Channel Negative Capacitance (GCNC) SOI MOSFET for Improved Device Performance and Temperature Resilience", in NANOfIM 2017 (Nanotechnology for Instrumentation and Measurement Workshop), held at Gautam Buddha University, Greater Noida, Uttar Pradesh, India, from November 16-17, 2017.

50 Monika Bansal and Harsupreet Kaur, "An analytical model for long channel Double Gate Ge Ferroelectric FET (DGGeFeFET) to study the impact of interface trap charges", presented (ORAL) in IEEE International Conference on Smart Technologies for Smart Nation (SmartTechCon 2017) held at Reva University, Bangalore, India, 17th-19th August 2017. Print ISSN: 978-1-5386-0570-7, Online ISSN: 978-1-5386-0569-1

51 Hema Mehta and Harsupreet Kaur, "Analytical Model to Study the Impact of Ferroelectric Materials SBT/PZT on Elliptical Gate All Around Junctionless Transistor", in IEEE TENSYMP 2017 –"Technologies for Smart Cities" to be held at Cochin, Kerala, India, from 14th-16th July, 2017.

52 Hema Mehta and Harsupreet Kaur, "High Temperature Performance Investigation of Elliptical Gate Ferroelectric Junctionless Transistor", (ORAL) in 3rd International Conference on Emerging Electronics (ICEE) 2016, held at IIT Bombay, Mumbai, India, 27th-30th December, 2016.

53 Monika Bansal and Harsupreet Kaur, "Analytical Threshold Voltage Model to study the impactof Graded-Channel (GC) design and gate dielectric engineering on device performance of Tri- Gate MOSFET", presented (ORAL) in International Conference on Recent Innovations in Engineering and Technology (ICRIEAT 2016), held at Hotel Katriya, Hyderabad, India, 22nd-23rd December 2016.

54 Hema Mehta and Harsupreet Kaur, "Analytical Model to Study Temperature Dependent Negative Capacitance Effect on Long Channel Double Gate Ferroelectric Junctionless Transistor", presented (POSTER) in Asia Pacific Microwave Conference (APMC) 2016, held at Hotel Pullman, Aerocity, New Delhi, India, 5th-9th December, 2016.

55 Hema Mehta and Harsupreet Kaur, "Analytical Drain Current Model to Study the Impact of

Negative Capacitance Phenomenon in Symmetric Double Gate Junctionless Transistor", presented (ORAL) in IEEE TENCON 2016 — Technologies for Smart Nation held at Marina Bay Sands, Singapore, 22nd-25th November, 2016.

56 Hema Mehta and Harsupreet Kaur, "Impact of Negative Capacitance phenomenon of Ferroelectric Materials SBT and PZT on Elliptical Gate All Around Junctionless Transistor", presented (POSTER) in International Conference on Advances in Nanomaterials and Nanotechnology (ICANN) 2016, held at Jamia Millia Islamia, New Delhi, I4th-5th November, 2016.

57 Hema Mehta, Harsupreet Kaur, "Modeling and Analysis of Double Gate Ferroelectric Junctionless (DGFJL) Transistor", IEEE Radio and Antenna Days of the Indian Ocean (RADIO) 2015, 21-24 September 2015, Mauritius.

58 Harsupreet Kaur, Hema Mehta, Analytical Modeling of Gate Oxide Engineered Junctionless SOI MOSFET with Vertical Gaussian-like Doping Profile, ICMARS 2014, 9-12 Dec 2014, Jodhpur, India.

59 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Laterally Asymmetric Channel and Gate Stack Design on Device Performance of Surrounding Gate MOSFETs: A Modeling and Simulation Study", Asia Pacific Microwave Conference, APMC 2008,16th -18th December 2008, Hong Kong.

60 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R.S.Gupta, "Asymmetric Multilayered GateDielectric (AMGAD) Surrounding gate MOSFET: A New Structural Concept for Improved Device Performance" Microwaves 2008, Jaipur, India.

61 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "A Comparative Analysis UsingModeling and Simulation to Study the Impact of Multilayered Gate Dielectric (MGD) Design on Device Performance of Surrounding Gate MOSFET", The XXIX General Assembly of the International Union of Radio Science (Union Radio Scientifique Internationale) URSI-2008, 9th - 16th August 2008, Chicago, Illinois, USA.

62 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Non-Uniformly Doped and Multilayered Asymmetric Gate Stack Design on Device Characteristics of Surrounding Gate MOSFETs", Workshop on Compact Modeling (WCM-2008), 1st -5th June, Boston, Massachusetts, U.S.A.

63 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Modeling and Simulation of Graded Channel Asymmetric Gate Stack (GCASYMGAS) Surrounding Gate MOSFET", Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed mode Applications, pp.43-44, 5th -6th January, 2008, New Delhi, India.

64 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Impact of Gate Stack Architecture on Device Characteristics of Surrounding Gate MOSFETs", Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed mode Applications, pp.45-46, 5th-6th January, 2008, New Delhi, India.

65 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Impact of Laterally AsymmetricChannel and Gate Stack Architecture on Device Performance of Surrounding Gate MOSFET (LACGAS SGT): A Simulation Study", International Semiconductor Device Research Symposium (ISDRS) 2007, pp.1892-1893, 12th -14th December, 2007, University of Maryland, USA

66 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "An Analytical Model for Graded Channel Asymmetric Gate Stack Surrounding Gate MOSFET (GCASYMGAS SGT)",

International Symposium on Microwave and Optical Technology (ISMOT) 2007, pp.817-820, 17th -21st December, Monte Porzio Catone, Italy.

67 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An analytical 2-Dimensional subthreshold model for drain induced barrier lowering (DIBL) effect in GaN MESFET", International Symposium on Microwave and Optical Technology (ISMOT ) 2007, 17th
- 21st December, Monte Porzio Catone, Italy.

68 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "A Two-Dimensional Analytical Model for I-V Characteristics of Graded Channel Surrounding Gate (GC SGT) MOSFET", International workshop on physics of semiconductor devices (IWPSD) 2007, pp.236-239, 16th - 18th December, Mumbai, India.

69 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Laterally Asymmetric Channel Gate Stack (LACGAS) SGT: A New Structural Concept for Improved Device Performance" International workshop on physics of semiconductor devices (IWPSD) 2007, pp.191-193, 16$^{th}$ 18th December, Mumbai, India.

70 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An Analytical Model for Admittance Parameters of GaN MESFET for microwave circuit applications" International workshop on physics of semiconductor devices (IWPSD) 2007, 16th -18th December, Mumbai, India

71 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Asymmetric Gate Stack Surrounding gate Transistor (ASYMGAS SGT): 2-D Analytical Threshold Voltage Model", Asia Pacific Microwave Conference (APMC 2007), pp. 2511-2514, 11th -14th December, Bangkok, Thailand.

72 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An analytical model for high temperature operation of GaN MESFETs" CODEC 2006, 18th -20th December, Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta "An Analytical Model of Sub-micron GaN MESFET's using Exact Velocity Field Dependence for Microwave Applications" IWPSD'2005, 13th -17th December, New Delhi, India.

73 Harsupreet Kaur, Sneha Kabra, Simrata Bindra, Subhasis Haldar and R.S.Gupta, "Modeling and Analysis of graded channel fully depleted cylindrical/ surrounding gate SOI MOSFETs", URSI 2005, 23rd -29th October, New Delhi, India.

74 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta "An Analytical Model for GaN MESFET's Using New Velocity-Field Dependence" International Conference on Nitride Semiconductors, ICNS'2005, 28th August-2nd September, Breman, Germany. Kolkata, India.

75 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An Analytical Threshold Voltage Model for Sub-Micron GaN MESFET" European Workshop on III Nitride Materials and Devices 2006, 18th-20th September, Crete, Greece.

76 Harsupreet Kaur, Sneha Kabra, Simrata Bindra, Subhasis Haldar and R.S.Gupta, "An Analytical 2- Dimensional Model for Graded Channel Fully Depleted Cylindrical/ Surrounding Gate SOI MOSFETs", International workshop on physics of semiconductor devices (IWPSD 2005), Vol.II, pp.1150-1155, 13th -17th December, New Delhi, India.

**NATIONAL CONFERENCES**

1. Hema Mehta and Harsupreet Kaur, "Theoretical Study of Impact of Ferroelectric Properties of SBT/PZT and Interface Layer on Double Gate Symmetric Junctionless Transistor", 2nd National Conference on Recent Developments in Electronics (NCRDE 2017), 17th-18th February 2017, Department of Electronic Science, University of Delhi South Campus, Delhi, India.
2. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "A Two-Dimensional Threshold Voltage Model for Graded Channel Fully Depleted Cylindrical/Surrounding Gate MOSFETs" MATEIT 2006, pp.259-262, 22nd -25th March, New Delhi, India.
3. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R.S.Gupta, "An Analytical Drain Current Model for Graded Channel Fully Depleted Cylindrical/Surrounding Gate MOSFET" Microwaves 2006, pp.116-118, 6th -8th October, Jaipur, India
4. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Graded Channel (GC) Design in Surrounding Gate MOSFET (SGT) for Improving Short Channel and Hot Carrier Performance", Indian Microelectronics Society (IMS) 2007, pp.216-220,16th -17th August, Chandigarh, India
5. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "A Two-Dimensional Threshold Voltage Model for Asymmetric Gate Stack Surrounding Gate MOSFET", MATEIT'2008, 26th -28th September, New Delhi, India.

BOOK CHAPTER

Negative Capacitance Field-Effect Transistors to Address the Fundamental Limitations in Technology Scaling", Harsupreet Kaur, Pages 187-202, Semiconductor Devices and Technologies for Future Ultra Low Power Electronics, CRC Press, 2021

INVITED TALKS DELIVERED/ SESSION CHAIR

1. Invited talk on "Polarity Controllable FETs – Emerging Prospect for Gas Sensing Applications", 10th International Conference on Microelectronics Circuits and Systems - Micro2023 held during July 1-3, 2023, Guwahati Assam and in online mode.
2. Invited talk on "Gaussian Doped Negative Capacitance Junctionless Transistors - Emerging Prospect for High Temperature Applications" – 7th World Engineering Conference on Contemporary Technologies – WECON - 2022, organized by Chitkara University, India on May 20-21, 2022.
3. Session Chair – 7th World Engineering Conference on Contemporary Technologies – WECON-2022, organized by Chitkara University, India on May 20-21, 2022.
4. Invited talk on "Introduction to VHDL and Applications" organized by Department of Electronics, Jammu University, March 2022.
5. Invited talk on "Negative Capacitance FETs – Emerging Prospect for Ultra Low Power Applications" - International Virtual Conference on Innovations in Science and Technology (IVCIST-2021) on 31st May 2021 organized by Nehru Arts and Science College (Autonomous), Coimbatore
6. Invited talk on "Ferroelectric Negative Capacitance Junctionless Transistors For Ultra Low Power Applications" - 8th International Conference on Microelectronics, Circuits and Systems (MICRO

2021) held during 08-09 May, 2021.

7. Invited talk on “Semiconductor Technology – Innovations, Current Trends and Challenges” in DBT sponsored seminar organized by Department of Physics, D.A.V College, Bhatinda on December 02, 2020 (Online mode)
8. Invited talk on "Emerging Nanoelectronic Devices" at Bhaskaracharya College of Applied Sciences, University of Delhi, on 20th February, 2019
9. Session Chair - Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2018 (ICMETE-2018) organised at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018.
10. Invited talk on “CMOS and VLSI Technology” at Hansraj College, University of Delhi, September 26, 2017.
11. Session Chair - International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2016) organised at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 22-23 September 2016.
12. Delivered following Invited talks at TEQIP-II Sponsored Faculty Development Programme on "Advances in Microelectronics and Plasma Diagnostics" (AMPD-2016), organized by Dept of Applied Physics, Delhi Technological University, August 29- September 2, 2016.
    a. CMOS Scaling: Review and Perspectives
    b. Material and Device Architecture Innovations for Advanced CMOS Technology

## PAPER PRESENTATION IN INTERNATIONAL/ NATIONAL CONFERENCES (2013 ONWARDS)

1. Presented a paper, " Effect of SBT Ferroelectric Layer on Polarity Controllable FETs for Improved Current Drivability", authored by Priyanka Pandey and Harsupreet Kaur IEEE 16$^{th}$INDICON 2019, Gujrat, 13-15Dec. 2019. (ORAL)
2. Presented a paper, "Enhanced Reliability of Polarity Controllable–Ferroelectric–FETs under the Impact of Fixed Trap Charges" authored by Priyanka Pandey and Harsupreet Kaur , Springer 3$^{rd}$International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, 28-29Sept. 2019. (ORAL)
3. Presented a paper, "Efficacy of Non-Uniformly Doped and Multi-layered Gate DielectricDesigns in Improving Device Perfomance of Elliptical MOSFETs" authored by Somishang Jagoi, Divya Pawar and Harsupreet Kaur, Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) held at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018 (ORAL).
4. Presented a paper, “Design Space Optimization for Nanoscale Graded Channel Negative Capacitance (GCNC) SOI MOSFET for Improved Device Performance and Temperature Resilience”, authored by Hema Mehta and Harsupreet Kaur in NANOfIM 2017 (Nanotechnology for Instrumentation and Measurement Workshop), held at Gautam Buddha University, Greater Noida, Uttar Pradesh, India, from November 16-17, 2017.(ORAL)
5. Presented a paper, "Hema Mehta and Harsupreet Kaur, “Analytical Model to Study the Impact of Ferroelectric Materials SBT/PZT on Elliptical Gate All Around Junctionless Transistor”, presented in IEEE TENSYMP 2017 – “Technologies for Smart Cities”, held at Cochin,Kerala, India, 14th-16th July, 2017(Oral presentation)
6. Presented a paper, "Modeling and Analysis of Double Gate Ferroelectric Junctionless (DGFJL) Transistor", authored by Hema Mehta and Harsupreet Kaur, IEEE Radio and Antenna Days of the Indian Ocean (RADIO) 2015, 21-24 September 2015, Mauritius. (Oral presentation)

## ORGANIZATION OF CONFERENCE (2013 ONWARDS)

1. Member- Technical Program Committee – International Conference on Emerging Technology and Sustainable Solutions (ICESS 2023) November 24-25, 2023, Chitkara University.
2. Co-Chair - 9th International Conference on Microelectronics, Circuits and Systems (MICRO 2022) held during 25-26 June, 2022, Jaipur, Rajasthan, India.
3. Co-Chair - 8th International Conference on Microelectronics, Circuits and Systems (MICRO 2021) held during 08-09 May, 2021 (ONLINE).
4. Member – Local Organizing Committee, 5th International Conference on Emerging Electronics (IEEE-ICEE 2020), held during 26-28 December 2020 (Virtual), IIT Delhi.
5. Co-Chair - 7th International Conference on Microelectronics, Circuits and Systems (MICRO 2020) jointly organized by Applied Computer Technology, Kolkata, India and Delhi Technological University, Delhi, India supported by IEEE EDS Delhi Chapter, 25-26 July, 2020 (Was held online).
6. Member - Abstract Registration Committee- International Conference on Renewable Energy & Emerging Technologies (ICREET – 2019), 13-14 November, 2019, Jakarta, Indonesia.
7. Member – Organizing Committee - Second national Conference on Recent Developments in Electronics (NCRDE-2017) held during 17-18 February 2017, at South Campus, Delhi University.
8. Member - Technical Program Committee - International Conference on Advances in Computers, Communication and Electronic Engineering (COMMUNE 2015) held at University of Kashmir, Srinagar during 16-18 March 2015.

## RESEARCH PROJECTS (MINOR)

1. Institution of Eminence (IoE), University of Delhi, 2021-2022, – Performance and Reliability Analysis of Advanced Gallium Oxide based Devices using Theoretical Framework and Simulations" (Rs. 5,00,000)
2. Institution of Eminence (IoE), University of Delhi, 2021-2022, Modeling, Design and Simulation of Novel Lateral $Ga_2O_3$ MOSFETs for Microwave Applications" (Rs. 3,00,000)
3. Institution of Eminence (IoE), University of Delhi, 2021, Investigation of Reconfigurable FETs for ultra low voltage/low power Ion-sensing and Immuno-sensing Applications and the impact of process and temperature variability on sensing performance" (Rs2,50,000)
4. DU R&D project titled, " Performance Evaluation of Elliptical Gate MOSFETs Using Analytical Modeling and Simulation" 2015-2016 (Rs. 2,70,000)
5. DU R&D project titled, " Modeling, Design and Simulation of Negative Capacitance Junctionless (NCJL) MOSFETs for ultra low power applications " 2014-2015 (Rs. 1,70,000)

## AWARDS AND DISTINCTIONS

1. Received International Travel Support from SERB – DST (Department of Science and Technology) for presenting paper, "Modeling and Analysis of Double Gate Ferroelectric Junctionless (DGFJL) Transistor", Hema Mehta and Harsupreet Kaur, IEEE Radio and Antenna Days of the Indian Ocean (RADIO) 2015, 21-24 September 2015, Mauritius. (Oral presentation)

2. Name listed in the *2010 edition of Who's Who in the World*
3. Won the 'Young Scientist Award' in The XXIX General Assembly of the International Union of Radio Science (Union Radio-Scientifique Internationale) URSI-GA 2008 conference held in Chicago, Illinois, USA during August 7-16, 2008.
4. Qualified CSIR-UGC NET and secured 7th rank in India.

**BEST PAPER AWARDS IN CONFERENCES**

- *Best paper award* - Priyanshi Goyal and Harsupreet Kaur, "Effect of Step Doping Profile and Dual Material Gate Design on β-$Ga_2O_3$ for superior RF Performance", IEEE 6th International Conference on Devices, Circuits and Systems (ICDCS) 21-22 April, 2022, 21 (pp. 6-10). IEEE
- *Best paper award* - Priyanka Pandey and Harsupreet Kaur, "Performance Assessment of Polarity Tunable– Ferroelectric–Field Effect Transistor at High Temperature —Part I", IEEE 5$^{th}$International Conference on Devices, Circuits and Systems (ICDCS -2020), held in Coimbatore, 5-6March, 2020.
- *Best paper award* **-** Monika Bansal and Harsupreet Kaur, "Study to Analyze the Impact of Fixed Trap Charges on the Performance of Germanium Ferroelectric Double Gate FET (GeFeDGFET)," IEEE International Conference On Computing, Power and Communication Technologies (GUCON), Greater Noida, Uttar Pradesh, India, 27th-28th September 2019.
- *Best paper award* **-** Monika Bansal and Harsupreet Kaur, "Superior Device Performance and Reliability of Germanium Ferroelectric Double Gate FET (GeFeDGFET) at High Temperatures",
  in NANOCON 2018 held at Bharati Vidyapeeth University, Pune-Satara Road Campus, Pune, India, 25$^{th}$-26$^{th}$ October 2018.
- *Best paper award* **-** Hema Mehta and Harsupreet Kaur, "Theoretical Study of Impact of Ferroelectric Properties of SBT/PZT and Interface Layer on Double Gate Symmetric JunctionlessTransistor", 2$^{nd}$ National Conference on Recent Developments in Electronics (NCRDE 2017), 17$^{th}$- 18$^{th}$ February 2017, Department of Electronic Science, University of Delhi South Campus, Delhi, India.

## REVIEWING

- IEEE Electron Devices Letters
- IEEE Transactions on Electron Devices
- IEEE Journal of the Electron Devices Society
- IEEE Access
- Solid State Electronics
- Silicon (Springer Nature)
- ECS-Journal of Solid State Science and Technology
- Integration (Elsevier)
- Nano-Micro Small (Wiley)
- Results in Physics
- AEU-International Journal of Electronics and Communications
- AIP Advances
- Nanoelectronics (Review Editor)
- Micromachines
- Microelectronics Journal

- Superlattices and Microstructures
- Japanese Journal of Applied Physics
- Journal of Electronic Materials
- International Journal of Numerical Modelling: Electronic Networks, Devices and Fields
- International Journal of Modelling and Simulation
- Optik – International Journal for Light and Electron Optics
- Journal of Electrical Engineering & Technology
- Reviewer - SERB DST proposals
- Reviewer for project proposals submitted to Executive board of Austrian Science Fund
- Reviewer -7th International Conference on Microelectronics, Circuits and Systems, to be held during 5th-6th June, 2020 at Delhi Technological University, India.
- Member – Abstract Committee – International Conference on Renewable Energy & Emerging Technologies, November 13, 2019, Jakarta, Indonesia
- Reviewer for international conference, IEEE NANOCON 2018 held during 25-26 October 2018, Pune.
- Reviewer for international conference, IEEE TENCON 2016 held during 22 - 25 November 2016, Marina Bay Sands, Singapore.
- Member - Technical Program Committee - International Conference on Advances in Computers, Communication and Electronic Engineering (COMMUNE 2015) held at University of Kashmir, Srinagar during 16-18 march 2015.

## MEMBERSHIP OF PROFESSIONAL BODIES

- Senior Member, IEEE USA (June 2018 – till date)
- Member, IEEE USA and Electronic Devices Society, USA
- Member, Member -IEEE Solid-State Circuits Society
- Life Member - Semiconductor Society of India

**Office Bearer-**

- Secretary - IEEE EDS Delhi Chapter (Jan 2020 – till date)
- Executive Member - IEEE-EDS Delhi Chapter (2013- till Dec2015)
- Executive Member - IEEE-EDS Delhi Chapter (Jan 2019- till date)
- Secretary - IEEE EDS Delhi Chapter (Jan 2020 – till date)

## CONFERENCES AND WORKSHOPS ATTENDED (2013 ONWARDS)

1. Attended IEEE 16thINDICON 2019, Gujrat, 13-15Dec. 2019.
2. Attended Springer 3rdInternational Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, 28-29 Sept. 2019.
3. Attended Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) organised at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018.
4. Attended Orientation Programme at Centre for professional Development in Higher Education, University of Delhi during June 08, 2018 - July 06, 2018.
5. Attended tutorial course on “III-N based RF devices” on December 11, 2017 in XIX International Workshop on the Physics of Semiconductor Devices (IWPSD 2017) organized by Solid State Physics Laboratory, Delhi and Indian Institute of Technology, New Delhi, December 11- 15, 2017.
6. Attended XIX International Workshop on the Physics of Semiconductor Devices (IWPSD 2017)

organized by Solid State Physics Laboratory, Delhi and Indian Institute of Technology, New Delhi, December 11-15, 2017.

7. Presented a paper, “Design Space Optimization for Nanoscale Graded Channel Negative Capacitance (GCNC) SOI MOSFET for Improved Device Performance and Temperature Resilience”, authored by Hema Mehta and Harsupreet Kaur in NANOfIM 2017 (Nanotechnology for Instrumentation and Measurement Workshop), held at Gautam Buddha University, Greater Noida, Uttar Pradesh, India, from November 16-17, 2017.(ORAL)
8. Presented a paper, ""“Analytical Model to Study the Impact of Ferroelectric Materials SBT/PZT on Elliptical Gate All Around Junctionless Transistor”, (ORAL) in IEEE TENSYMP 2017 – “Technologies for Smart Cities”, held at Cochin, Kerala, India, 14th-16th July, 2017
9. Presented a paper, "Hema Mehta and Harsupreet Kaur, Modeling and Analysis of Double Gate Ferroelectric Junctionless (DGFJL) Transistor", IEEE Radio and Antenna Days of the Indian Ocean (RADIO) 2015, 21-24 September 2015, Mauritius.
10. International Mini Workshop on VLSI systems, Jawaharlal Nehru University, New Delhi, Jan12th -13th, 2015.

## TALKS/ WORKSHOPS/ LECTURES ORGANIZED (2013 ONWARDS)

1. IEEE EDS DL Talk on “Predictive Analytics in Machine Learning” by Dr. Rajiv Joshi, IBM, T. J. Watson Research Center, on March 13, 2023 at University of Delhi South Campus.
2. Technical talk under the aegis of the centenary celebration of the University of Delhi by Prof. Ajit Panda, NSIT Berhampur on the topic “5G Electronics systems” on Fenruary 03, 2023.
3. Workshop to commemorate the centenary celebration of University of Delhi on the topic "Emerging Devices, Circuits and Systems", November 15 - 18, 2022.
4. Committee member - Research Conclave for Research Scholars Of Department of Electronic Science, University of Delhi" on October 15, 2022 at University of Delhi South Campus.
5. IEEE Distinguished Lecture on “Spintronics-Perspectives and Challenge” by Prof. Brajesh Kaushik, IIT Delhi on10th February, 2022.
6. Distinguished Alumni Lecture Series – Talk on “Role of Science and Technology in the Development of Society” by Sh. Raj Singh, Scientific Officer – H, Institute for Plasma Research, Gandhinagar on 13th January, 2022.
7. Distinguished Alumni Lecture Series – Talk on “TV White Space technology: Opportunities and Challenges” by Sh. Pankaj Sharma, Senior Manager, Institute of Microelectronics (Agency for Science, Technology & Research) & Co-Founder, Whizpace) on 9th December, 2021.
8. IEEE EDS Distinguished Lecturer talk on “Differentiated Silicon for Non-terrestrial Broadband Internet addressing the digital divide” by Dr. Anirban Bandyopadhyay, Senior Director, Strategic Applications, GLOBALFOUNDRIES, Inc., USon 12th November, 2021.
9. IEEE EDS Distinguished Lecturer talk on “3D Integration: above and beyond Moore’s law” Prof. Jesús A. del Alamo, Massachusetts Institute of Technology, 29th October, 2021.
10. Distinguished Alumni lecture Series – the following two talks were organized, (a) Talk on "Application of GaN based devices in RF Electronics“ by Dr. Meena Mishra, SSPL, DRDO. (b) Talk on "Microwaves in medical fields including neutralizing COVID-19 virus" by Prof. K. P. Ray, DIAT, Pune on 22nd October, 2021.

11. IEEE EDS Distinguished Lecturer talk was organized on “Nanoelectronics to nanotechnology : More Moore and more than Moore” by Prof. Durga Misra, New Jersey Institute of Technology (NJIT), Newark, USA on 20th October, 2021.
12. Distinguished Alumni lecture Series – the following two talks were organized, (a) Talk on “Antennas for RF Energy harvesting system design” by Dr. Nasimuddin, Scientist, SRO, Institute for Infocomm Research, A*STAR (b)Talk on "Phased array and Gimbel version seekers" by Dr. Yogesh Verma, Head - AD & AESA Seekers Division, Research Centre Imarat, DRDO Hyderabad on 29th September, 2021.
13. Webinar on PCB Manufacturing and Assembly – the following three talks were organized, (a) Talk on “Electronics Manufacturing Industry in India” by Mr. Vinit Verma, Director PROSEM Technology India Pvt. Ltd. (b) Talk on “An Introduction to PCB Manufacturing and Assembly” by Dr. Hema Mehta Kapoor, Director (Operations and Management), HMPCB Solutions,
14. (c)Talk on “ Process Flow and Virtual Tour of PCB and PCBA Unit” by Ms. Monika Bansal, Director (Circuit Design and Technical Support), HMPCB Solution on 7th September, 2021.
15. Coordinator - IEEE Electron Devices Society DL Mini Colloquium (Virtual) on "Emerging Nano Devices and Circuits – The Roadmap Ahead" Jointly organized by Department of Electronic Science, University of Delhi South Campus and IEEE EDS Delhi Chapter, October 05-09, 2020 (Virtual)
16. IEEE-EDS Technical Lecturer Talk by Professor Cher Ming Tan, Chang Gung University, Taiwan on “Computational Reliability – A paradigm shift in product reliability assurance” at University of Delhi South Campus, New Delhi on January 28, 2020.
17. Coordinator – “Workshop on VLSI Current Trends Using Mentor Graphics & Xilinx” jointly organized by Department of Electronic Science University of Delhi South Campus and CoreEL TECHNOLOGIES (Technically sponsored by IEEE EDS Delhi Chapter) on 21-22 March, 2018 at University of Delhi South Campus.
18. Coordinator – Visitors’ Program organized by Department of Electronic Science, University of Delhi South Campus, sponsored by IEEE EDS Delhi Chapter and IEEE MTT-S Student Branch Chapter, IIT Delhi on March 12, 2016 at University of Delhi South Campus.
19. IEEE-EDS Technical Lecturer Talk by Dr. Amitava Sen Gupta, Scientist- H, Time and frequency standards department, National Physical Laboratory on “Atomic Clocks- How do they work and why do we need them?” at University of Delhi South Campus, New Delhi on November 14, 2014.

**Other Information:**

1. Resource person & Judge in interdisciplinary workshop “New Frontiers in Science” organized by Acharya Narendra Dev College on 22 October 2019.
2. Judged the Hardware projects organized for students of Delhi-NCR by Project WIE Stand, IEEE WIE Delhi Section on 29 April 2017 at University of Delhi, South Campus.
3. Mentored a student, Sundaram Yadav, student of B.Tech (Electronics) of Acharya Narendra DevCollege for the Summer Internship Programme in Laboratory Research organized by CIC-Centrefor Science Education and Communication during June - July 2016.